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Robert A. Manware

Sir:

## REPLY BRIEF

This Reply Brief is being filed in response to the Examiner's Answer mailed on March 21, 2007.

Appellant files this Reply Brief to address certain statements made by the Examiner in the Examiner's Answer. First, Appellant will address the Examiner's statements regarding the grounds of rejection, and specifically the rejections of independent claims 41, 54 and 62. Secondly, Appellant will address certain statements made by the Examiner in the "Response to Arguments" section of the Examiner's Answer.

First, the Examiner has rejected claims 41, 42, 45, 48-49, 51, 53-55, 58-60, 62-65 and 67 under 35 U.S.C. § 103(a) in view of Arai (U.S. Patent No. 5,280,599) and Yoshizawa (U.S. Patent No. 5,787,464). However, not only do the references fail to disclose each of the recited elements, the Examiner has not shown the requisite motivation or suggestion to combine the cited references to reach the present claims. In contrast, the Examiner has picked statements among isolated disclosures in the prior art to deprecate the claimed invention. Throughout the

Examiner's arguments, the Examiner has presented numerous conclusory statements based on various portions of the references without providing any indication of their context, nor any support as to how the cited references may be combined. Accordingly, Appellant feels it would be best to provide a brief overview of the technologies addressed in the references before addressing the Examiner's arguments.

The Examiner relies primarily on two references, Arai and Yoshizawa. Arai is directed generally to a computer with a memory expansion function, and more particularly to a computer system suitable for an expansion memory that may be used in expanded and extended memory configurations. As explained in Arai, early PC systems incurred limitations due to the ability of some processors to address a minimal amount of memory. For instance, some systems were not designed to access memory locations in excess of one megabyte (MB). In response to these limitations, developers employed various techniques to increase the amount of memory that could be accessed, including "extended memory" and "expanded memory." As illustrated in Arai, extended memory includes memory with addresses greater than or equal to one megabyte. A visual representation is provided by the dashed area in FIG. 1 of Arai. Access to the extended memory is generally limited and may require running applications in certain modes to access the memory address above one megabyte. Expanded memory is memory addressed from within the lower one megabyte of memory space, typically between 640kB and the upper 1MB, and referred to as a "page frame," as illustrated in FIG. 1 of Arai. With expanded memory, the system uses the page frame as a window to accesses additional memory addresses. In other words, the system can access a memory address space of one megabyte or more through the window. Arai also discusses a third configuration that includes a combination of expanded and extended memory, and discusses various issues of the combination, including the possibility that multiple devices trying to access the memory addresses and the potential for destroying contents in extended and expanded memory locations. *See* Arai, col. 2, ll. 6-40.

Accordingly, the objective of Arai is to "provide a computer system which permits desired expanded and extended memory configurations to be set easily without the occurrence of malfunctions." Id. at col. 2, ll. 42-45. The basic method of operation disclosed in Arai includes having an operator specify a desired one of the first, second and third memory arrangements and

its memory capacity (the memory capacity of each of the expanded and extended memories) from a keyboard. Id. at col. 4, ll. 18-22. The data on the capacities of the expanded and extended memories are stored in memory control registers and based on the capacities, the system sets the expanded and extended memory arrangements. Id. at col. 4, ll. 32-34; col. 4, ll. 41-45; FIG. 5. As a result, a desired extension memory arrangement can be set without troublesome operation or the misuse of memory. Id. at col. 5, ll. 9-17. In other words, an operator inputs information regarding the desired allocation of expanded and extended memory, and the computer system uses this information to set the extended memory, expanded memory or a combination arrangement. *See* Arai, FIG. 5.

The second reference relied on by the Examiner, Yoshizawa, discloses "a computer system and method for enabling memory expansion without shutting off the computer." *See* Yoshizawa, Abstract. Yoshizawa identified a limitation in the prior art where systems that do not have an open memory slot required the system to be shut off before a memory device could be swapped out. Id. at col. 1, ll. 28-35. The disclosed invention of Yoshizawa "enables memory expansion without shutting off the system for computer systems that do not have an open memory slot by replacing the installed memory with a memory with a larger capacity." Id. at col. 1, ll. 38-41. For instance, Yoshizawa discloses the OS determining that a memory extraction/insertion event occurs, comparing the inserted memory capacity to the capacity of another system, updating an internal table, and either copying information to the memory or not based on the size of the inserted memory. *See* Yoshizawa, col. 3, ll. 12-52; *See* FIG.3A. In other words, the system detects changes in the installed memory and swaps data between the installed memories to enable "hot-swapping" of a memory device into a memory slot without any user interaction, other than physically changing out the memory device.

Turning now to the Examiner's arguments, Appellant would like to address two claim limitations discussed by the Examiner. Specifically, Appellant will discuss the Examiner's arguments on page 8-9 of the Examiner's Answer regarding the claim limitation of "executing a software routine to determine a maximum number of memory devices that can be supported per memory bus channel of the computer system," followed by a discussion of the arguments on page

5-8 of the Examiner's Answer regarding the claim limitation of "determining memory upgrade options based on the determined memory capacity of the computer system."

Before discussing the lack of motivation or suggestion to combine the references in the manner recited in the present claims, Appellant believes it is important to direct attention to two preliminary issues. First, the Examiner stated that the Appellant "conceded" that the claim limitation of "executing a software routine to determine a maximum number of memory devices that can be supported per memory bus channel of the computer system," was a "well known technique" based on statements Appellant made on page 10 of the Appeal Brief; however this was not the case. The Examiner has taken the statement of "readily understood by one of ordinary skill in the art" out of context and has manipulated the description to conveniently fit the Examiner's argument. In fact, when read in context, the statement "readily understood by one of ordinary skill in the art" clearly refers to the preceding portion of the statement relating to reading information from a non-volatile storage device. Accordingly, Appellant asserts that prefacing the Examiner's arguments with this limitation was improper. Appellant does not concede that the aforementioned claim limitation in well known and in fact Appellant traverses such an assertion.

Second, in light of the Examiner's arguments that continue to focus on the elements of the claims, Appellant notes that examination of the claims reveals a deficiency relating to the recitations in claims 41, 54 and 62 including "determining a maximum number of memory devices that *can* be supported per memory bus channel" and "determining a maximum number of device sockets that *can* be supported by a memory controller" (emphasis added). Accordingly, the recited claims provide for determining the potential capabilities of the system and not simply determining the current amount of memory installed and functioning based on that determination, as taught by the cited references. None of the references cited by the Examiner discloses the claimed features, nor do they make the claimed limitations obvious. For instance, as discussed previously, the Arai reference is directed to allocating the *installed* memory in accordance with instructions provided by an operator. As disclosed, the system prompts an operator for input relating to allocation of the memory as expanded or extended memory, and executes a routine to allocate the *installed* memory based on the selections of the operator. Further, Yoshizawa does not obviate this deficiency. In fact, Yoshizawa bases its actions on the actual memory that was

previously *installed* or is currently *installed*. For instance, as described previously, Yoshizawa stores information of a memory device removed from a socket and compares that information to similar information relating to a subsequently installed device. Further, the Examiner relies on RAMUS as extrinsic evidence of the recited limitation. However, the Examiner merely discusses RAMBUS in the context of determining whether a device is present or not. Further, the RAMBUS data sheet relied on by the Examiner fails to teach or suggest any configuration that indicates the maximum number of device sockets that *can* be supported by the memory controller. In other words, the claims recite determining a number of memory devices or sockets that can be supported by the system and, in contrast, the Arai reference discloses merely allocating memory based on the memory that is actually installed in the system, Yoshizawa merely discloses a system and method of swapping installed memory, and RAMBUS merely addresses what is currently installed. None of the three references determine the potential capabilities of the system, but instead are based on what is actually installed in the system. Accordingly, the references relied on by the Examiner fall short of providing the recited limitation of determining the number of memory devices or memory sockets that "can" be supported by a memory bus channel or a memory bus controller.

Returning now to the Examiners basis for the rejection of independent claims 41, 54 and 62, a *prima facie* case of obviousness has not been established for the § 103 rejections. Appellant notes that even if all of the claimed limitations were found to exist in the prior art, there is no suggestion or motivation to combine the references. As discussed above, the Arai reference generally relates to a technique to allocate a known memory capacity between an expanded and extended memory based on inputs of an operator. In contrast, Yoshizawa is concerned with the providing a technique to physically remove a memory device from a socket and replace that memory device with a second memory device without having to shutdown the system during the device swap. Accordingly, even assuming that the references provide each of the recited claim limitations, the difference in their purpose and methods of operation provides no motivation to combine the teachings of the Arai reference with the Yoshizawa reference to reach the claimed limitations. Further, in light of the Examiner's reference to the RAMBUS datasheet, Appellant notes that although the designer of Arai's computer system may have known the maximum numbers when the system was designed, there is no teaching or motivation in implementing the

determination of these maximum numbers in software or in a software routine, as there is no reason why Arai's system or processor of this system would execute such software during operation to derive this information. Similarly, the system of Yoshizawa is concerned with enabling swapping of memory devices into an existing memory location and has no suggestion or motivation to determine the maximum number of memory devices or device sockets that can be supported. Accordingly, the Examiner has failed to provide a *prima facie* case of obviousness for independent claims 41, 54, and 62.

Next, Appellant's discussion focuses of the arguments on page 5-8 of the Examiner's Answer regarding the claim limitation of "determining memory upgrade options based on the determined memory capacity of the computer system." First, Appellant notes that the Examiner prefaced his arguments by stating that the Examiner has given the broadest meaning to the term "upgrade options"; however, following this statement, the Examiner failed to give any deference to the claim limitation. In fact, the Examiner's arguments focus entirely on portions of the claims related to determining the memory capacity of the computer system and do not provide any argument relating to the claim limitation of "determining memory upgrade options." For instance, the Examiner initially states that the memory address space of Arai is "not necessarily in the context of memory devices per se," and followed by a brief discussion of known address space limitations. Based on the discussion, the Examiner draws the conclusion that these "teachings and showings confirm that Arai teaches the feature of the last clause of claims 41, 54 and 62 of determining memory upgrade options based on the determined memory capacity of the computer system.'" However, the Examiner has provided no discussion regarding "determining memory upgrade options." Subsequent to this statement, the Examiner again states that "Arai alone has no explicit teaching of relating these expansion abilities to memory devices per se." Presumably, the Examiner is equating "expansion abilities" to the previously described technique of allocating between expanded and extended memory to work around the one megabyte limitation. Therefore, the Examiner recognizes this feature being absent from Arai.

In an attempt to resolve this limitation, the Examiner suggests that Yoshizawa makes "explicit" what has been "implied" by Arai's teachings. Examiner's Answer, p. 7. Specifically, the Examiner suggests that the "insertion and extraction" of memory modules in Yoshizawa

"clearly dovetails" with the expansion abilities of Arai. Appellant respectfully disagrees. As discussed previously, Arai discloses allocating between expanded and extended memory within a system and does not teach or suggest swapping memory modules. Further, Arai does not even contemplate or require swapping memory modules as taught by Yoshizawa. First, all of the elements of the claims are not present and, second, there is no teaching, suggestion or motivation to combine these references. The Examiner merely provides conclusory statements as to the desirability of combining the Arai and Yoshizawa references and has failed to provide any objective evidence as to why one of ordinary skill in the art would combine the references. Accordingly, the Examiner has failed to provide a *prima facie* case of obviousness for independent claims 41, 54, and 62.

Finally, Appellant takes the opportunity to addresses the "Response to Arguments" section of the Examiner's Answer. First, the Examiner stated that "[s]ome of the appealed claims are simply combinations of prior claims that which the Board of Patent Appeals and Interferences has already considered." Examiner's Answer, p. 11. Appellant respectfully disagrees. For instance, the Examiner contends that "appealed claim 54 is a combination of the features of previous claim 32 and claim 30." However, previously considered independent claim 32 recites:

> [a] program storage device, readable by a programmable control device, comprising instructions for causing the programmable control device to: obtain memory configuration information of a computer system, the computer system including memory devices; determine a memory capacity for the computer system; and determine memory upgrade options to replace one or more the memory devices based on a residual memory capacity of the computer system.

Prior dependent claim 30 recites:

> [t]he method of claim 21, wherein the act of determining a memory capacity comprises obtaining an indication of a maximum number of memory module sockets for the computer system.

Present independent claim 54 recites:

> [a] program storage device, readable by a programmable control device, comprising instructions for causing the programmable control device to: obtain memory configuration information of a computer system; determine a memory capacity for the computer system, including determining a maximum number of device sockets *that can be supported by a memory controller of the computer system*; and determine memory upgrade options based on the determined memory capacity of the computer system. (emphasis added)

It should be noted that prior claim 30 is dependent on prior claim 21 and, therefore, was not previously considered in combination with prior independent claim 32. However, even if taken in combination, independent claim 54 recites determining the maximum number of device sockets that *can* be supported by a memory controller of the computer system, which is not a limitation recited by prior claims 30 and 32. Appellant points out that the closest combination of prior claims may actually include prior claims 32 and 34. However, even this combination fails to recite all of the claim limitations recited by present independent claim 54. Accordingly, Appellant contends that the Examiner's arguments regarding prior combinations are incorrect.

Appellant also points the Board of Patent Appeals and Interferences to inconsistencies in the Examiner's evaluation of the prior and present claims. For instance, in the Examiner's Answer, the Examiner stated that "the presently appealed claims are merely a combination of the previous independent claims with various previous dependent claims – *all of which fell with the affirmation of the rejections of August 31, 2004*." However, immediately following this statement, the Examiner conceded that two of the three independent claims, 41 and 62, include a new limitation that has not been decided by the Board of Patent Appeals and Interferences. Examiner's Answer, p. 12. Specifically, the Examiner notes the limitation of "executing a software routine to determine a maximum number of memory devices that can be supported per memory bus channel of the computer system." This statement alone indicates that the independent claims 41 and 62 and their dependent claims 42-51, 53, 63-65 and 67 have not been considered previously by the Board of Patent Appeals and Interferences. Accordingly, Appellant respectfully contends that the Examiner's statements are at best conclusory and are in fact completely inconsistent with the Examiner's own observations and statements.

Second, Appellant respectfully disagrees with the Examiner's consideration of the additional claim limitation previously discussed, which includes "executing a software routine to determine a maximum number of memory devices that can be supported per memory bus channel of the computer system." The Examiner again attempts to read a concession on the part of the Appellant into his argument. Specifically, the Examiner states that "in an attempt to overcome the previous rejections under 35 U.S.C. 112, first paragraph, appellant explicitly admitted that using

this technique to determine total memory capacity in prior art computer systems and was 'readily understood by one of ordinary skill in the art.'" However, similar to the discussion above the Examiner has again taken the statement of "readily understood by one of ordinary skill in the art" out of context and has manipulated the description to conveniently fit the Examiner's argument. In fact, when read in context, the statement "readily understood by one of ordinary skill in the art" clearly refers to the preceding portion of the statement relating to reading information from a non-volatile storage device. Accordingly, Appellant feels that prefacing the Examiner's arguments relating to this limitation was improper.

**Conclusion**

Based upon the above points of clarification in conjunction with the arguments made in the Appeal Brief, Appellant believes that the claims are clearly allowable over the cited art. The Examiner's rejections, therefore, cannot stand.

Respectfully submitted,

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Robert A. Manware
Reg. No. 48,758
FLETCHER YODER
P.O. Box 692289
Houston, TX 77269-2289
(281) 970-4545